CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A decoder for driving a wordline, comprising:

a latch set to a particular state when said wordline is to be driven;

a decoding circuit for receiving and decoding the address of said wordline and setting said latch to said particular state; and,

a first output inverter, comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being sent to said particular state.

2. The decoder of claim 1, further comprising:

a voltage pump for supplying a voltage to said first output inverter which drives said selected wordline with a pumped voltage.

3. The decoder of claim 1, further comprising:

a second output inverter, connected to the output of said first output inverter and comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being sent to said particular state.

4. The decoder of claim 2, further comprising:

a voltage sink, connected to said first output inverter, said voltage sink being at a potential lower than ground.

5. The decoder of claim 4, wherein said voltage pump and voltage sink shift the output levels of said inverter between said pumped voltage and said potential lower than ground.

6. A processor circuit, comprising

a processor; and

a memory circuit for exchanging data with said processor;

at least one of said processor and memory circuit comprising a wordline decoder, said decoder comprising:

a latch set to a particular state when said wordline is to be driven;

a decoder for receiving and decoding the address of said wordline and setting said latch to said particular state; and,

an output inverter, comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being sent to said particular state.

7. The decoder of claim 6, further comprising:

a voltage pump for supplying a voltage to said output inverter which drives said selected wordline with a pumped voltage.

8. The decoder of claim 7, further comprising:

a voltage sink, connected to said output inverter, said voltage sink being at a potential lower than ground.

9. The decoder of claim 8, wherein said voltage pump and voltage sink shift the output levels of said inverter between said pumped voltage and said potential lower than ground.

10. The decoder of claim 6, further comprising:

a second output inverter, connected to the output of said first output inverter and comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being sent to said particular state.

11. An method of operating a wordline decoder, comprising:

decoding wordline address information and setting a latch associated with a wordline to a predetermined state when an address of said wordline is decoded; and

driving said selected wordline with an first output inverter having an input connected to an output of said latch.

12. The method of claim 11, further comprising:

supplying a voltage from a voltage pump to turn on said wordline.

13. The method of claim 11, further comprising:

supplying a voltage sink to turn off said wordline.

14. The method of claim 11, further comprising:

driving said selected wordline with a second output inverter having an input connected to an output of said first output inverter.

15. The method of claim 11, further comprising:

choosing a size of a pair of cross-coupled transistors within said latch so as to minimize power consumption.

16. The method of claim 14, further comprising:

choosing the size of a pair of complementary transistors within said first output inverter to have maximum switching speed while still minimizing their power consumption.